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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,539	01/12/2004	Takuji Matsumoto	247561US2	8827

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EXAMINER	
HUYNH, ANDY	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 05/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/754,539	TAKUJI ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 9-11* is/are rejected.

7)☒ Claim(s) *2 and 4-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/02/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-11** are currently pending in the application is acknowledged.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in JAPAN, 2003-006641 on 01/15/2003 and 2003-295234 on 08/19/2003.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 04/02/2004. The references cited on the PTOL 1449 form have been considered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1, 3, 9, 10 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al. (USP 6,314,021 hereinafter referred to as "Maeda") in view of Chau et al. (USP 6,765,273 hereinafter referred to as "Chau").

Regarding claims **1 and 3**, Maeda discloses in Fig. 36 and the corresponding texts as set forth in column 17, line 10-column 22, line 67, a semiconductor device/a high-voltage circuit portion comprises:

an SOI substrate 1 having a semiconductor substrate 2, an insulating layer 3, and a semiconductor layer of a first conductivity type 4 that are stacked in this order;

element isolation insulating films 5 formed partially in a main surface of said semiconductor layer, with portions of said semiconductor layer interposed between said insulating layer and bottom surfaces of said element isolation insulating films;

a gate structure 13 formed partially on said main surface of said semiconductor layer in an element formation region defined by said element isolation insulating films; and

source/drain regions 14 have a second conductivity type that is different from said first conductivity type, said source/drain regions forming a pair, with said channel formation region interposed therebetween, and having bottom surfaces or depletion layers that reach said insulating layer.

Maeda fails to teach or suggest a semiconductor device/a high-voltage circuit portion comprises a pair of recesses formed in said element formation region, said recesses being formed in said main surface of said semiconductor layer in portions that are not covered by said gate structure, with a channel formation region under said gate structure interposed between said pair of recesses; and source/drain regions formed in bottom surfaces of said recesses; wherein each said recess is positioned beneath said gate structure. However, Chau teaches in Figs. 2-3I that an integrated circuit 200 includes a pair of recesses 332 formed in an element formation region, said recesses being formed in a main surface of a semiconductor layer in portions that are not covered

by a gate structure 208, with a channel formation region under said gate structure interposed between said pair of recesses; and source/drain regions 222 formed in bottom surfaces of said recesses, and each said recess is positioned beneath said gate structure (Figs. 2 and 3F). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of forming a pair of recesses in an element formation region, and said recesses being formed in a main surface of a semiconductor layer in portions that are not covered by a gate structure, with a channel formation region under said gate structure interposed between said pair of recesses; source/drain regions formed in bottom surfaces of said recesses, and each said recess is positioned beneath said gate structure, as taught by Chau, into and modify the Maeda's structure to arrive the claimed limitations in order to provide increased margins for preventing silicide encroachment over the isolation region as set forth in column 6, lines 49-52.

Regarding claim 9, Maeda discloses the claimed invention except for the semiconductor device further comprises semiconductor regions formed on the bottom surfaces of said recesses; and metal-semiconductor compound layers formed on said semiconductor regions. Chau teaches in Figs. 4A-4B the semiconductor device comprises semiconductor regions 400 formed on the bottom surfaces of said recesses 332; and metal-semiconductor compound layers 336 formed on said semiconductor regions. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form semiconductor regions on the bottom surfaces of said recesses; and metal-semiconductor compound layers formed on said semiconductor regions, as taught by Chau in order to enable the manufacture of "raised" source/drain regions which reduce resistances of the device and improve performance as set forth in column 8, lines 33-56.

Regarding claims **10-11**, Maeda discloses in Fig. 36 the SOI substrate comprises an NMOS transistor/a first transistor operating at a relatively low power-supply voltage and a PMOS transistor/a second transistor operating at a relatively high power-supply voltage that are formed therein, and said semiconductor device is said NMOS transistor or said PMOS transistor; and said semiconductor device is said first transistor or said second transistor.

Allowable Subject Matter

Claims **2, 4, 5, 7 and 8** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Regarding claim **2**, the prior art of record, taken alone or in combination, fails to teach or suggest the semiconductor device wherein the part of the main surface of the semiconductor layer where the gate structure resides forms an angle larger than 90° with a side surface of each of the recess; regarding claims **4 and 5**, the prior art of record, taken alone or in combination, fails to teach or suggest the semiconductor device wherein a depth from said main surface of said semiconductor layer to said bottom surface of each said recess is smaller than a depth from said main surface of said semiconductor layer to a bottom surface of each said first impurity-introduced region as recited in claim **4**; regarding claim **6**, the prior art of record, taken alone or in combination, fails to teach or suggest the semiconductor device wherein said source/drain regions comprise third impurity-introduced regions formed in said main surface of said semiconductor layer, wherein a depth from said main surface of said semiconductor layer to bottom surfaces of said third impurity-

introduced regions is greater than a depth from said main surface of said semiconductor layer to bottom surfaces of said first impurity-introduced regions, and wherein a depth from said main surface of said semiconductor layer to said bottom surfaces of said recesses is smaller than a depth from said main surface of said semiconductor layer to said bottom surfaces of said third impurity-introduced regions; regarding claims 7 **and 8**, the prior art of record, taken alone or in combination, fails to teach or suggest the semiconductor device wherein said gate structure comprises second sidewalls formed on said bottom surfaces of said recesses and in contact with said first sidewalls as recited in claim 7.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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05/03/05

Andy Huynh

Patent Examiner